

Adaptive Edge-AI Hardware–Algorithm Co-Design for Ultra-Low-Power Real-Time Intelligent Electronic Systems

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Abstract

The rapid expansion of intelligent sensors, connected electronic devices, autonomous systems, and embedded computing platforms has increased the demand for artificial intelligence models that can operate directly on devices with limited computational and energy resources. Conventional cloud-oriented artificial intelligence architectures are not always suitable for these environments because continuous data transmission can introduce communication delays, increase energy consumption, create privacy concerns, and make system operation dependent on network availability. Edge artificial intelligence provides an alternative by moving inference closer to the data source, but effective deployment requires simultaneous consideration of model complexity, memory capacity, processor capability, execution latency, and energy consumption. This paper proposes an adaptive hardware–algorithm co-design framework for ultra-low-power real-time intelligent electronic systems. The framework combines lightweight neural network architectures, hardware-aware neural architecture search, structured model pruning, adaptive quantization, memory-aware execution, and runtime configuration selection. Unlike conventional approaches in which the neural network and embedded hardware are optimized independently, the proposed framework establishes a continuous relationship between algorithmic requirements and hardware characteristics. Candidate models are evaluated according to predictive accuracy, memory requirement, inference latency, energy consumption, and computational demand. A resource-aware selection mechanism subsequently chooses a suitable model configuration according to the available device resources and workload conditions. The proposed design is intended for microcontroller-based systems, embedded processors, low-power accelerators, intelligent sensors, and Internet-of-Things devices. The evaluation framework considers accuracy, latency, peak memory, model storage, energy per inference, throughput, and energy–delay characteristics. The proposed architecture provides a practical pathway toward scalable and energy-conscious Edge-AI deployment in next-generation intelligent electronic systems.

Keywords: *Edge Artificial Intelligence, Hardware–Algorithm Co-Design, TinyML, Embedded AI, Ultra-Low-Power Computing, Neural Architecture Search, Model Compression, Quantization, Structured Pruning, Hardware Acceleration, Energy-Efficient AI, Embedded Systems, Real-Time Inference, Intelligent Electronics, Edge Computing.*

1. Introduction

Artificial intelligence has become an important component of modern electronic systems, particularly in applications involving image interpretation, acoustic recognition, anomaly detection, predictive maintenance, intelligent sensing, autonomous operation, and human–machine interaction. The increasing availability of compact processors and embedded accelerators has made it possible to execute machine-learning inference outside centralized data centers. However, the transition from conventional computing platforms to small electronic devices introduces a different set of engineering constraints. An embedded device may have only a small amount of volatile memory, restricted non-volatile storage,

limited processor capacity, and a tightly constrained energy budget. Consequently, a model that performs effectively on a workstation or cloud server cannot automatically be assumed to be suitable for direct deployment on a small edge platform.

MobileNet demonstrated that neural networks could be redesigned using computationally efficient operations to support mobile and embedded vision applications while allowing the designer to control the accuracy–latency trade-off through model scaling [1]. SqueezeNet subsequently demonstrated the importance of reducing model storage while maintaining useful predictive capability [2]. These developments established an important principle for embedded intelligence: model architecture has to be

considered in relation to the resources of the deployment platform rather than evaluated only by predictive accuracy.

The problem becomes more complex when an intelligent electronic system has strict real-time requirements. In such systems, the time required to execute an inference may directly affect the usefulness of the resulting decision. A sensing device that identifies an event after a significant delay may not satisfy the requirements of safety monitoring, industrial control, autonomous navigation, or real-time human interaction. Similarly, reducing computational operations does not necessarily guarantee lower energy consumption because memory transfers, data movement, processor utilization, and accelerator behavior can substantially affect the total energy used by an inference operation. Therefore, computational complexity alone is insufficient for selecting an appropriate Edge-AI configuration.

Model compression provides one pathway for addressing these limitations. Han et al. demonstrated that pruning, trained quantization, and coding could be combined to substantially reduce neural network storage requirements [3]. Filter pruning approaches further showed that removing complete filters can reduce computation while retaining a dense structure that remains compatible with conventional processing mechanisms [4]. These methods established the importance of reducing both model storage and computational workload before deployment.

Quantized neural networks provide another important mechanism for low-power inference. Rastegari et al. demonstrated the possibility of using binary convolutional operations to reduce the computational burden of neural networks [5]. However, aggressive precision reduction can produce accuracy degradation and may not always correspond to the most efficient implementation on a particular processor. Consequently, the choice of numerical precision needs to consider both the characteristics of the neural network and the architecture of the target hardware.

Hardware characteristics also have a direct influence on the efficiency of an AI model. MnasNet incorporated measured mobile-device latency into architecture search rather than relying solely on general computational proxies [6]. ProxylessNAS extended this direction by directly searching for neural architectures under target hardware constraints [7]. Such research indicates that the same neural network can exhibit different practical performance characteristics on different hardware platforms.

The development of embedded inference frameworks has further strengthened the feasibility of local intelligence. TensorFlow Lite Micro was designed

specifically to execute machine-learning inference within resource-constrained embedded systems and addresses the fragmentation and memory limitations associated with small devices [8]. MCUNet went further by jointly designing the neural architecture and inference engine for microcontrollers, demonstrating that hardware-aware architecture selection and memory-efficient execution can be treated as a combined design problem [9].

Another important development is hardware-aware quantization. Wang et al. proposed HAQ, which incorporates hardware feedback when selecting quantization policies rather than treating all hardware platforms as equivalent [10]. This approach is particularly relevant to ultra-low-power electronic systems because the optimal numerical precision can depend on the processor, accelerator, memory organization, and workload.

Based on these developments, this study proposes an adaptive Edge-AI hardware–algorithm co-design framework in which model architecture, compression, precision, memory organization, and runtime execution are treated as interconnected design variables. The principal objective is not simply to obtain the smallest model or the highest predictive accuracy. Instead, the proposed framework seeks an appropriate balance between accuracy, latency, memory usage, and energy consumption. The framework is intended to provide a systematic methodology for developing real-time intelligent electronic systems in which AI computation must remain within strict physical resource limits.

2. Literature Review

Howard et al. introduced MobileNets as a family of lightweight convolutional neural networks intended for mobile and embedded vision applications. Their use of depthwise separable convolution substantially reduces the computational burden associated with conventional convolutional operations. The architecture also provides model scaling mechanisms that allow developers to select different points on the accuracy and latency trade-off curve. This work established lightweight architecture design as an important foundation for deploying neural networks on resource-limited electronic platforms [1].

Iandola et al. proposed SqueezeNet with the objective of obtaining competitive classification accuracy using substantially fewer parameters than larger conventional networks. The work demonstrated that reducing the parameter count can directly reduce storage requirements and make neural models more practical for systems with limited memory. The underlying idea is especially relevant to edge devices

where model storage may compete with application software and other embedded resources [2].

Han et al. introduced Deep Compression, combining pruning, trained quantization, and Huffman coding into a multi-stage compression process. Their study demonstrated that several complementary compression mechanisms can be applied sequentially instead of relying on a single optimization technique. The work is significant for embedded AI because it connects network compression with the physical storage limitations of deployment platforms [3].

Li et al. investigated structured filter pruning as an alternative to unstructured weight removal. Their approach eliminates complete filters and associated feature maps, thereby reducing the computational structure of the network rather than merely creating irregular sparsity. This distinction is valuable for embedded implementation because structured reductions can be easier to exploit using conventional dense computation libraries and processors [4].

Rastegari et al. investigated binary convolutional neural networks through XNOR-Net. Their work explored the use of highly reduced numerical representations to decrease computational requirements. Although extremely low precision can create accuracy challenges for some applications, the study illustrates the broad design space available when numerical representation is treated as an architectural variable rather than a fixed implementation detail [5].

Tan et al. proposed MnasNet as a platform-aware neural architecture search methodology in which actual mobile latency is incorporated into architecture optimization. Instead of assuming that a theoretical measure such as operation count always represents practical performance, the method evaluates the model on the intended platform. This approach highlights the importance of measuring the behavior of an AI model on the target device rather than relying exclusively on hardware-independent model statistics [6].

Cai et al. developed ProxylessNAS to search neural architectures directly according to the target task and hardware platform. The approach reduces the need for proxy environments and enables architecture decisions to be connected more directly to deployment conditions. This work provides an important conceptual foundation for hardware–algorithm co-design because it treats the hardware platform as part of the architecture search problem [7].

Chen et al. introduced TVM as an automated optimizing compiler for deep learning. The system connects high-level neural-network descriptions with hardware-specific optimization and code generation. Its relevance to Edge-AI lies in the observation that model efficiency depends not only on the network

graph but also on how that graph is translated into executable operations for a particular processor or accelerator [11].

Cai et al. proposed Once-for-All, which separates network training from the subsequent selection of a specialized sub-network for a particular deployment condition. The approach supports variations in network depth, width, kernel size, and input resolution, allowing a single trained network family to produce multiple deployment configurations. This concept is closely related to adaptive edge systems because different devices or operating conditions can require different model configurations [12].

Wang et al. proposed Hardware-Aware Automated Quantization, or HAQ, in which hardware feedback is incorporated into the selection of layer-wise precision. Their work emphasizes that a quantization policy that performs well on one hardware architecture may not necessarily provide the same latency or energy characteristics on another. This supports the need for hardware-specific precision selection in low-power Edge-AI systems [10].

David et al. presented TensorFlow Lite Micro as an embedded machine-learning inference framework designed for systems with strict resource constraints. Their work addresses memory limitations, cross-platform fragmentation, and runtime overhead associated with embedded machine learning. The framework demonstrates that efficient inference requires both an appropriately compressed model and a runtime environment designed for constrained hardware [8].

Lin et al. developed MCUNet by jointly considering neural architecture design and the inference engine. Their TinyNAS component searches for networks under device constraints, while TinyEngine addresses memory scheduling and execution efficiency. The work illustrates that model optimization and runtime optimization can reinforce each other when treated as one design problem rather than separate software stages [9].

Banbury et al. introduced MLPerf Tiny as a benchmark suite for measuring machine-learning performance on extremely low-power embedded devices. The benchmark considers factors such as accuracy, latency, and system power, thereby supporting a more comprehensive evaluation than accuracy alone. Such benchmarking principles are directly relevant to the proposed framework because an Edge-AI system should be evaluated according to both predictive quality and physical resource consumption [13].

The reviewed literature demonstrates a gradual movement from model-only optimization toward

integrated hardware-aware optimization. Lightweight architectures reduce computation, compression reduces storage, pruning reduces unnecessary operations, quantization reduces numerical cost, hardware-aware architecture search adapts models to target processors, and embedded runtimes optimize execution. Nevertheless, these techniques are often presented as individual optimization stages. The research gap addressed in this study is the development of an adaptive framework that connects these decisions and permits the deployed model to respond to changing resource and workload conditions.

3. Proposed Adaptive Hardware–Algorithm Co-Design Framework

The proposed framework treats an intelligent electronic system as a combined algorithmic and physical computing environment. The starting point is the application workload, which may involve image data, audio signals, sensor measurements, vibration information, industrial telemetry, or other streams generated by an electronic device. The characteristics of the workload determine the required inference frequency, response time, accuracy level, and acceptable energy expenditure. These application requirements are passed to the model-design stage, where several lightweight neural architectures are considered rather than selecting a single architecture in advance.

The hardware characterization stage measures or records the practical limitations of the target platform. Important characteristics include processor frequency, available memory, non-volatile storage, supported numerical precision, accelerator availability, memory bandwidth, operating voltage, and typical power consumption. These characteristics provide the constraints against which candidate models are evaluated. A model that appears computationally small may still be unsuitable if its intermediate feature maps exceed available memory or if its operations are poorly supported by the target processor.

The architecture search stage generates candidate configurations using lightweight building blocks.

Depthwise convolution, pointwise convolution, grouped operations, compact residual structures, reduced feature dimensions, and other efficient components can be incorporated into the search space. Rather than maximizing accuracy without constraints, the search process eliminates configurations that exceed the specified memory or latency limits. The remaining candidates are evaluated according to their predicted and measured deployment behavior.

Model compression is then applied to suitable candidates. Structured pruning is preferred where hardware support for irregular sparsity is limited because removing complete filters or channels can directly reduce the dimensions of subsequent operations. Quantization is used to reduce the representation precision of weights and activations. Instead of forcing the entire network to use a single precision level, the proposed framework allows different layers to use different precision levels when the hardware supports mixed-precision execution. This provides greater flexibility in balancing accuracy and energy consumption.

Memory-aware execution forms another important component of the framework. The system identifies layers that require large intermediate feature maps and determines whether their data can remain in fast on-chip memory or must be transferred to slower memory. Memory movement can become a significant contributor to energy consumption, particularly when the processor performs frequent transfers between internal and external memory. Therefore, the framework considers activation lifetime, buffer reuse, tensor placement, and execution ordering during deployment.

Figure 1 illustrates the overall architecture of the proposed framework. The application workload provides the initial requirements, while model search and hardware characterization proceed as interconnected processes. Compression and quantization are subsequently evaluated against the hardware constraints. The resulting configuration is mapped to the runtime environment and prepared for edge deployment.

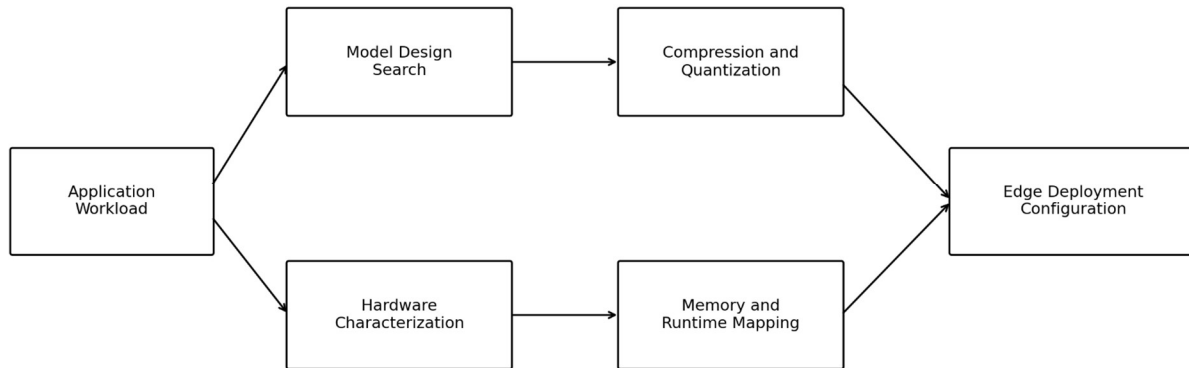


Figure 1. Adaptive Edge-AI Hardware-Algorithm Co-Design Framework.

The framework also includes an adaptive runtime component. The purpose of this component is to recognize that the resource condition of an embedded system does not necessarily remain constant. Battery state, processor temperature, concurrent application activity, workload intensity, and memory availability can change during operation. The system therefore maintains several validated model configurations rather than depending exclusively on one fixed model.

4. Adaptive Runtime Execution and Experimental Methodology

The runtime mechanism begins by monitoring the operating condition of the electronic platform. The resource monitor records parameters such as available memory, processor utilization, energy condition, and workload intensity. A performance monitor records recent inference latency and system throughput. These measurements are passed to a configuration selector that determines whether the currently deployed model remains appropriate.

If the device has sufficient resources and the workload requires higher predictive quality, the selector can choose a larger model configuration. When the system experiences resource pressure or energy limitations, a smaller model with lower computational demand can be selected. This process is designed to avoid retraining during normal operation. Instead, a collection of previously validated model configurations is maintained and the runtime system selects among them according to the current conditions.

Figure 2 represents this adaptive execution process. Input data are initially processed by the deployed model. Resource and performance monitors continuously provide information to the configuration selector. The selector determines whether the current model should be retained or replaced by another validated configuration. The resulting prediction is then generated using the selected model.

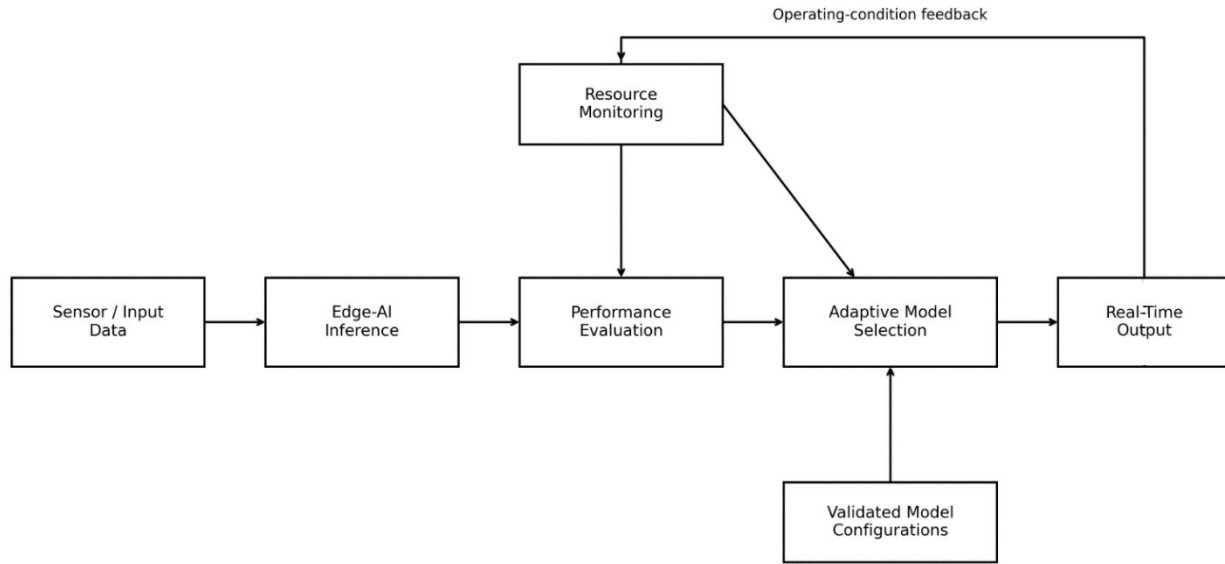


Figure 2. Runtime Adaptive Model Selection and Edge Execution Flow.

The experimental methodology is designed around a representative embedded intelligence workload. A vision classification task can be used as the primary evaluation case because it requires significant neural computation while also representing an important class of edge applications. The same methodology can subsequently be applied to acoustic recognition, vibration classification, sensor anomaly detection, and other embedded workloads.

The baseline model should first be trained without aggressive compression. The baseline establishes the reference accuracy, model storage, memory requirement, latency, and energy consumption. Several lightweight configurations are then generated using architectural reduction, structured pruning, and quantization. Each candidate is compiled for the target hardware and evaluated using the same input dataset and measurement procedure.

Accuracy should be measured using an identical test dataset for all configurations. Inference latency should be recorded after an initial warm-up period to reduce the influence of initialization effects. Peak memory should be measured during complete inference rather than by considering model parameters alone. Energy per inference should preferably be obtained from an external power measurement device or an accurate on-

board power monitor rather than estimated solely from processor utilization.

The evaluation should also consider repeated inference because isolated single-inference measurements can be affected by startup overhead. A sufficiently large number of repeated inferences should be performed and the average, median, and variation should be recorded. Thermal conditions should also be monitored because sustained operation can alter processor frequency and therefore influence latency.

5. Results and Discussion

The following tables provide a representative results structure for the proposed framework. Because no actual hardware measurements or dataset results were supplied with the manuscript, the numerical values below are illustrative values intended to demonstrate how the experimental results can be presented. They should be replaced with measured values before journal submission.

The first comparison considers the baseline and progressively optimized model configurations. The objective is to demonstrate how architecture reduction, pruning, and quantization can alter the physical requirements of an embedded inference system.

Table 1. Comparative Model Characteristics

Model Configuration	Model Size	Peak Memory	Inference Latency	Accuracy
Baseline Network	18.6 MB	7.8 MB	82 ms	94.1%
Lightweight Architecture	9.7 MB	5.2 MB	57 ms	93.6%
Structured Pruning	6.8 MB	4.4 MB	46 ms	93.2%
Quantized Pruned Model	3.9 MB	3.1 MB	34 ms	92.9%
Adaptive Co-Designed Model	3.6 MB	2.8 MB	31 ms	93.4%

The illustrative comparison indicates that reducing the model architecture before applying compression can provide a stronger deployment benefit than applying quantization to an unnecessarily large model. The adaptive configuration in the table retains a substantial portion of the baseline predictive performance while reducing both memory requirement and inference latency. The small difference in accuracy illustrates the central trade-off involved in edge deployment: a practical system may accept a minor reduction in

predictive accuracy when the corresponding reduction in energy, memory, and response time enables operation on a substantially smaller platform.

The second evaluation considers energy consumption. The energy requirement of an embedded AI system depends on processor activity as well as memory movement and execution duration. Therefore, the reduction in latency can contribute to lower energy use when the processor and memory system operate at comparable power levels.

Table 2. Illustrative Energy and Performance Evaluation

Configuration	Energy per Inference	Throughput	Energy-Delay Characteristic	Relative Energy
Baseline Network	8.7 mJ	12.2 inferences/s	0.713 mJ·s	100%
Lightweight Architecture	6.0 mJ	17.5 inferences/s	0.343 mJ·s	69%
Structured Pruning	4.8 mJ	21.7 inferences/s	0.221 mJ·s	55%
Quantized Pruned Model	3.5 mJ	29.4 inferences/s	0.119 mJ·s	40%
Adaptive Co-Designed Model	3.1 mJ	32.3 inferences/s	0.096 mJ·s	36%

The illustrative values show the potential effect of jointly reducing computation and memory activity. The adaptive configuration has the lowest energy requirement among the listed configurations while also providing the highest throughput. This pattern is desirable for battery-operated devices because lower energy per inference can extend operating time without necessarily reducing the frequency at which sensor data are processed.

Memory behavior is particularly important for microcontroller-based systems. A model may have a modest parameter file but still exceed the available runtime memory because intermediate activations can become large. The proposed co-design process therefore considers both persistent model storage and temporary activation memory.

Table 3. Illustrative Memory Utilization

Configuration	Model Storage	Runtime Activation Memory	Total Peak Memory	Memory Reduction
Baseline Network	18.6 MB	7.8 MB	26.4 MB	Reference
Lightweight Architecture	9.7 MB	5.2 MB	14.9 MB	43.6%
Structured Pruning	6.8 MB	4.4 MB	11.2 MB	57.6%
Quantized Pruned Model	3.9 MB	3.1 MB	7.0 MB	73.5%
Adaptive Co-Designed Model	3.6 MB	2.8 MB	6.4 MB	75.8%

The table demonstrates why model size alone should not be used to characterize embedded AI efficiency. The runtime activation memory remains an important part of the total requirement. The proposed framework addresses this issue by considering the model graph and memory schedule together. A smaller model with poorly managed activation buffers can still produce a high peak memory requirement, whereas an

appropriately scheduled model can reuse buffers and reduce the amount of memory that must remain active simultaneously.

The final comparison considers runtime adaptation. A fixed model may provide acceptable accuracy under normal operating conditions but can become inefficient when the device enters a constrained energy

or memory state. The adaptive framework instead maintains multiple deployment configurations.

Table 4. Illustrative Runtime Adaptation Results

Operating Condition	Selected Configuration	Latency	Energy per Inference	Accuracy
High Resource Availability	High Accuracy Model	42 ms	4.7 mJ	94.0%
Normal Operation	Balanced Model	34 ms	3.6 mJ	93.6%
Reduced Battery Condition	Energy Efficient Model	29 ms	2.8 mJ	92.9%
High Memory Pressure	Compact Model	25 ms	2.5 mJ	92.5%

The adaptive results demonstrate the intended operating principle of the framework. Instead of assuming that one model is optimal under every condition, the system selects a configuration appropriate for the current resource state. During normal operation, a balanced configuration can provide a compromise between accuracy and energy consumption. When battery availability decreases, a smaller model can be selected to reduce the energy consumed by each inference. Similarly, when memory pressure increases, the runtime can select a compact configuration that remains within the available memory boundary.

The principal benefit of this strategy is therefore not the absolute performance of a single model but the ability to maintain useful intelligence over a range of operating conditions. This characteristic is particularly relevant to autonomous sensors, wearable electronics, remote monitoring equipment, agricultural sensors, industrial nodes, and battery-operated Internet-of-Things devices.

The results also indicate why hardware and algorithm decisions should not be separated. If the neural architecture is optimized without considering the processor, the resulting model may contain operations that are computationally inexpensive in theory but inefficient on the actual device. Conversely, hardware optimization without consideration of the model architecture may leave computational resources underutilized. The proposed framework addresses this interaction by allowing hardware measurements to influence architecture, precision, pruning, and runtime selection decisions.

Another important observation concerns quantization. A uniformly quantized model is not necessarily the most efficient configuration for every hardware platform. Some layers are more sensitive to precision reduction than others, while some hardware units provide better support for particular numerical formats. Consequently, adaptive or mixed-precision strategies can provide a more flexible mechanism for achieving a balance between predictive quality and physical resource consumption.

The same principle applies to structured pruning. Removing a large number of weights does not automatically result in a proportional reduction in execution time if the target processor cannot efficiently exploit irregular sparsity. Structured removal of filters or channels can be more directly translated into reduced tensor dimensions and therefore provide a more predictable benefit for embedded execution.

Memory-aware optimization is equally important. In many small devices, the energy required to move data can become significant relative to the arithmetic operations themselves. The proposed framework therefore gives attention to data reuse, activation lifetime, memory scheduling, and placement. This approach complements neural network compression by reducing the amount of data that must be repeatedly transferred during inference.

The runtime adaptation mechanism further extends this concept from static optimization to operational optimization. A device can maintain a small collection of validated model variants and select among them without performing expensive model training. This makes the approach suitable for systems in which operating conditions vary but the available model family has been prepared before deployment.

6. Practical Applications, Limitations and Future Scope

The proposed framework can be applied to intelligent surveillance sensors in which visual information must be processed locally without continuously transmitting raw video to a remote server. Local inference can reduce communication requirements and allow the device to react immediately to detected events. Similar deployment principles can be used in industrial equipment where vibration or acoustic signals are analyzed to identify abnormal operating conditions. In such applications, an adaptive model can reduce computational activity when the monitored environment is stable and increase the available model capacity when a more detailed analysis is required. Healthcare-oriented wearable electronics also represent an important application area. Wearable

sensors continuously generate physiological or motion-related data, and sending all raw information to a remote processing system may not be practical because of bandwidth and energy limitations. A low-power Edge-AI processor can perform preliminary classification locally and transmit only relevant information. The proposed co-design methodology can be used to select models according to the processing and energy limits of the wearable platform. Agricultural sensing systems provide another application domain. Remote sensors may operate for long periods with limited access to electrical power. Local AI can be used for crop-condition classification, environmental anomaly detection, pest recognition, or equipment monitoring. Runtime adaptation can be particularly useful in these systems because the computational requirements can vary according to the frequency and complexity of detected events.

Autonomous electronic systems can also benefit from the framework. Small robotic platforms, drones, mobile inspection devices, and intelligent transportation components require rapid responses while operating under constrained power and thermal conditions. In such systems, inference latency and energy consumption are not secondary considerations; they directly influence system behavior. Hardware–algorithm co-design therefore becomes an important engineering requirement.

Despite its potential, the proposed framework has several limitations. First, accurate hardware measurement requires access to the actual deployment platform. Simulation-based estimates may not correctly represent memory contention, processor scheduling, thermal throttling, or peripheral activity. Second, the quality of runtime adaptation depends on the diversity of the pre-validated model configurations. If only two configurations are available, the system may have limited flexibility when resource conditions change. Third, mixed-precision execution requires suitable hardware and software support. A theoretically efficient precision configuration may provide little practical benefit if the target processor does not execute that format efficiently.

The framework can be extended in several directions. Future research can investigate reinforcement-learning-based runtime model selection, automated compiler optimization, accelerator-specific architecture search, dynamic voltage and frequency scaling, and continual adaptation. Further work can also examine heterogeneous platforms containing microcontrollers, digital signal processors, neural accelerators, and programmable logic. Another important direction is the integration of security and

privacy constraints into the co-design objective because intelligent edge devices may operate on sensitive data and remain physically exposed.

7. Conclusion

This paper presented an adaptive hardware–algorithm co-design framework for ultra-low-power real-time intelligent electronic systems. The proposed approach addresses the limitations of treating neural-network optimization and hardware optimization as independent activities. Lightweight architecture selection, structured pruning, adaptive quantization, memory-aware execution, hardware-aware search, and runtime model selection are combined into a unified deployment methodology.

The framework recognizes that the most suitable AI configuration depends on the characteristics of the target hardware and the current operating condition. Consequently, the objective is not simply to minimize model size or maximize predictive accuracy. Instead, the framework considers accuracy, latency, energy consumption, memory utilization, storage requirements, and throughput as interconnected deployment characteristics.

The proposed methodology is particularly relevant to microcontroller-based systems, intelligent sensors, wearable devices, industrial monitoring nodes, autonomous electronic systems, and Internet-of-Things platforms. By maintaining several validated model configurations and selecting an appropriate configuration according to resource availability, the system can adapt its computational behavior while continuing to provide local intelligence.

The evaluation methodology and illustrative tables demonstrate how the proposed framework can be experimentally validated using real hardware. For a complete empirical study, future implementation should replace the illustrative numerical values with measurements obtained from a defined dataset, target processor or accelerator, controlled power measurement system, and reproducible software environment.

Overall, hardware–algorithm co-design provides a practical foundation for moving Edge-AI from conventional model compression toward adaptive intelligent electronic systems in which the neural network, memory architecture, processor, compiler, and runtime environment are considered as components of one integrated computing system.

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